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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/207,745	12/08/1998	DANIEL S. SIMPKINS	32172-143271	7213

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WASHINGTON, DC 200439998

EXAMINER

TRAN, PHUC H

ART UNIT	PAPER NUMBER
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2664

DATE MAILED: 11/30/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

MLC

Office Action Summary

Application No.

09/207,745

Applicant(s)

SIMPKINS ET AL.

Examiner

PHUC H TRAN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 September 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 8-14 is/are rejected.
- 7) ☒ Claim(s) 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 and 8-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kosuge et al. (U.S. Patent No. 4575844).

- With respect to claim 1, Kosuge teaches a switch for switching time division multiplexed data and packet data from input ports to output ports (e.g. Fig. 1 shows the basic system configuration of a digital switching system for circuit and packet through TDM), which comprises: a plurality of input ports receives data (e.g. terminals in Fig. 1), wherein each data comprises either TDM data or packet data (e.g. the line 15 shows the TDM input data in Fig. 1); a plurality of output ports transmits switched data (e.g. terminals in Fig. 1); and a shared memory (e.g. hierarchical storage in Fig. 1) couples the input ports to the output ports; the shared memory sequentially receives the data from the input ports (e.g. the shared memory sequences receiving in input line 15); the shared memory switching sequentially receives data from a respective input port to a respective output port (e.g. the shared memory sequences outputting data on output line 16), wherein switching of packet data by the shared memory has no latency or jitter effect on switching of TDM data by the shared memory (see col. 2, lines 11-25).

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- With respect to claim 2, Kosuge also teaches each data is received by an input port as a time slot in a frame (e.g. the time slots in Fig. 3 for each data input into the switch).

- With respect to claim 3, Kosuge further teaches the shared memory, which comprises a TDM data memory portion (e.g. CKT switching call buffer in Fig. 1) and a packet data memory portion (packet switching call buffer in Fig. 1).

- With respect to claim 4, Kosuge discloses the shared memory that treats the input ports as logical input ports (e.g. the input port in Fig. 1 as terminals).

- With respect to claim 5, Kosuge teaches the shared memory places sequentially received packet data in a queue for a respective output port (e.g. data is received at the switch memory to transmit to the output).

- With respect to claim 6, Kosuge also teaches the data are received by the input ports and transmitted by the output ports as data exchange units (e.g. the system of Kosuge as exchange unit to transmit data from input to output port).

- With respect to claim 8, Kosuge teaches the switching of a data from a respective input port to a respective output port is controlled by a stored switch configuration (it is inherently to know the control section 14 in Fig. 1 for control the switching of data from input to output).

- With respect to claim 9, Kosuge also teaches an input data router sequentially routing data from the input ports to the shared memory; and an output data router sequentially routing data from the shared memory to the output (e.g. Fig. 1 shows the sequentially routing data from the input to the shared memory and to the output).

- With respect to claims 10 & 13, Kosuge teaches switching time division multiplexed data and packet data from input ports to output ports (e.g. Fig. 1 shows the basic system

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configuration of a digital switching system for circuit and packet through TDM), which comprises the steps of: switching a TDM data from an input port to an output port that comprises the steps of: receiving a TDM data at the input port (e.g. terminals in Fig. 1); determining the output port to route the TDM data (e.g. the data is routing and determining the output port at the control); storing the TDM data in a preselected area of a shared memory (e.g. the data is stored in CKT switching call buffer in Fig. 1); reading the TDM data from the shared memory (e.g. the control section reads the data from memory); transmitting the TDM data from the output port (e.g. terminals in Fig. 1); and switching a packet data from an input port to an output port, which comprises the steps of: receiving a packet data at the input port (e.g. terminals in Fig. 1); determining the output port to route the packet data; storing the packet data in the shared memory (e.g. the packet data is stored in packet switching call buffer in Fig. 1); reading the packet data from the shared memory (e.g. the control memory reads out data from the memory); and transmitting the packet data from the output port (e.g. terminals in Fig. 1); wherein switching packet data has no latency or jitter effect on switching TDM data (see col. 2, lines 11-25).

- With respect to claim 11, Kosuge discloses the preselected area of memory for storing the TDM data is based on a time slot in a frame (e.g. the hierarchical storage in Kosuge's invention).

- With respect to claim 12, Kosuge also teaches the output port to which the TDM data is routed is determined based on a time slot in a frame in which the TDM data was received by the input port, and wherein the output port to which the packet data is routed is determined based on routing data embedded in the packet data and based on the input port which received the packet

data (e.g. the data from input ports is determined to send to the output ports base on the times and the destination information).

- With respect to claim 14, Kosuge discloses wherein the data are received by input ports and transmitted by the output ports as data exchange units (e.g. the system of Kosuge as exchange unit to transmit data from input to output port). The data exchange units for packet data comprise routing information (e.g. the digital switching units 10 in Fig. 1 are for routing information from one terminal to another). The switching of a data exchange unit from a respective input port to a respective output port is controlled by a stored switch configuration (it is inherently to know the control section 14 in Fig. 1 for control the switching of data from input to output). The stored switch configuration uses the routing information of data exchange units for packet data to determine respective output port to switch the data exchange units (e.g. the control section is for controlling and routing the information through the digital switch unit).

Response to Arguments

3. Applicant's arguments with respect to claims 1-6, & 8-14 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Howells et al. (U.S. Patent No. 3732548) discloses switching center for a data network.
- Key et al. (U.S. Patent No. 6119215) discloses synchronization and control system for an arrayed processing engine.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUC H TRAN whose telephone number is (703) 308-7471. The examiner can normally be reached on M-F (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WELLINGTON CHIN can be reached on (703) 305-4366. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 872-9314.

Phuc Tran
Assistant Examiner
Art Unit 2664

P.t
November 15, 2001



Ricky Ngo
Primary Examiner
Art Unit 2664